REMARKS/ARGUMENTS

Reconsideration of the application is respectfully requested for the following reasons:

Amendment to Claims

Claim 2 has been amended to improve claim language. Furthermore, previously presented Claim 14 has been rewritten as the new Claim 21 in independent form including all of the limitations of base claim 9 and allowable claim 11. Claims 21 through 24 are newly added. No claims are cancelled. It is respectfully submitted that the changes are clearly supported by the application as filed, and therefore do not constitute new matter.

Claim Objections

Claim 2 is objected to because of informalities. In response, Applicant has amended claim 2 according to the Examiner's suggestion.

CLAIM REJECTION-35 U.S.C. SECTION 102 (b)

Rejection of Claims 1-2, 4-7, 9-10, and 12-13 under 35 U.S.C. 102(e) as being anticipated by Song et al (U.S. Patent No. 6,635,532).

This rejection is respectfully traversed on the basis that Song et al does not disclose "a buried conductive region between said plurality of isolation regions" as claimed. It is well settled that a "claim is anticipated only if each and every elements as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).

The Examiner is of the opinion that Song et al disclosed a structure of nonvolatile memory array. As to claim 1, the recitations "a buried conductive region between said plurality of isolation regions, wherein said buried conductive region is perpendicular to each of said plurality of isolation regions" and "a plurality of gate structures on said substrate except on said buried conductive region" are not disclosed in Song et al

Song et al does not disclose the recitation "a buried conductive region between said plurality of isolation regions, wherein said buried conductive region is perpendicular to each of said plurality of isolation regions" of claim 1. Song et al merely discloses the common source line is exposed along one direction and is formed self-aligned with the respective word lines WL. Referring to FIG. 11B of Song et al, the common source line is **under** the field oxide layer (115), which is not "**between** said plurality of isolation regions".

Furthermore, in the claimed invention, there is no isolation region in the source line, and the depth of the source region is smaller than the depth of the isolation. But, in col. 5, lines 46-47, Song et al shows the common source line 113a is deeper than the conventional flash memory cell. Hence, the claimed invention is not anticipated by Song et al.

Moreover, the claimed invention requires that the "depth of the buried conductive region" be "**smaller** than the isolation region". However, Song et al discloses the portion of the common source line is under the field oxide layer, that is, the depth of the common source line is **larger** than the field oxide layer. Thus, the buried conductive region is formed at different positions in the substrate. Therefore, Song et al cannot anticipate the claimed invention.

Rejection of Claims 1-5 and 7-8 under 35 U.S.C. 102(b) as being anticipated by Lee et al (U.S. Patent No. 6,211,012).

This rejection is also respectfully traversed for the similar reason that Lee et al does not disclose "a buried conductive region between said plurality of isolation regions" as claimed.

The Examiner is of the opinion that Lee et al disclosed a structure of nonvolatile memory array. Lee et al disclosed that "each source array has a plurality of source regions separately positioned between device isolation lines". The Examiner alleges that the buried conductive region (such as source region), which is not visible from the figures of Lee et al, is nevertheless located between said plurality of isolation regions. Applicant submits that Lee et al did not disclose "a plurality of gate structures on said substrate except on said buried conductive region" as claimed. Moreover, Lee et al did not specify that the "depth of the buried conductive region" is "smaller than the isolation region" as claimed. From the figures of Lee et al, the depth of the drain region might be smaller than the isolation device, but the depth of the source region cannot be visually compared with that of the isolation region. Thus, Lee et al cannot anticipate the claimed invention.

New claims 21-24 include the indicated allowable subject matter of claim 11 and should be allowed.

Conclusion

In the light of the above amendments and remarks, Applicant respectfully submits that all pending claims 1 though 13 and 21 through 24 as currently presented are in condition for allowance. Applicant has thoroughly reviewed the art cited but not relied upon by the Examiner. Applicant has concluded that these references do not affect the patentability of the claims as currently presented. Accordingly, reconsideration and allowance are respectfully requested.

The Examiner is invited to telephone the undersigned, Applicant's attorney of record, to facilitate advancement of the present application.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 07-1337 and please credit any excess fees to such deposit account.

Respectfully submitted,

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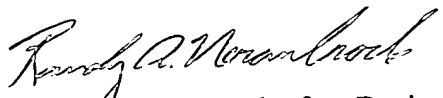

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